

Course Schedule - Spring 2008

Electrical and Computer Engineering

462 **Logic Design** credit: 3 hours.

Design of combinational networks, hazards, finite state machines, design of sequential networks in fundamental mode and pulse mode, state reduction, state assignment and races, and fault detection and testing. Same as CS 462 and MATH 491. Prerequisite: ECE 290 or CS 231.

CRN	Type	Section	Time	Days	Location	Instructor
33957	discussion-recitation	C	10:00 AM - 11:20 AM	MW	room 101 Transportation Bldg	Vasudevan, S
33957: 3 hours						